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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,541		03/10/2000	Maarten A. Koning	11283/9	5215
26646	7590	01/14/2004		EXAMINER	
KENYON & KENYON				BANANKHAH, MAJID A	
ONE BROADWAY NEW YORK, NY 10004				ART UNIT	PAPER NUMBER
	,			2127	a
			DATE MAILED: 01/14/2004	1	

Please find below and/or attached an Office communication concerning this application or proceeding.

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)

Attachment(s)

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_ 5) Notice of Informal Patent Application (PTO-152)

6) Other:

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- 1. This final office action in response to paper number 8, request for reconsideration that was filed October 14, 2003. Claims 1-21 are presented for examination. Applicants' argument has been fully considered but they are not deemed to be persuasive.
- 2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior Office action.
- 3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mateosian (Operating System Support- The Z8000 Way, Computer Design, May 1982).

As per claims 1, 14, 17-18, Mateosian et al. ("699") teach:

- memory Space (memory, Fig. 1), a task (Fig, 3), a first task control block associated with the task and located in a first area of the memory space (Fig. 3, process manager), the first task control block including a number of first task information data structures that contain first task information (Fig.3, schedule, lock/unlock, suspend/resume, and create/destroy);

a second task control block associated with the task and located in a second area of the memory space (Fig. 3, event/queue manager, memory management, and Interrupt/Trap Handler), the second task control block including a number of second task

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information data structures that contain second task information (create/destroy, queue/dequeue, and wait/test/signal);

wherein the first area of the memory space is not directly accessible by the task, and the second area of the memory space is directly accessible by the task (The program status area pointer control registers and the system mode stack register are all inaccessible from normal mode [See: process manager and system status, such as suspend/resume, and lock/unlock], and normal mode stack register is accessible from system mode, page 256, Right col. Lines 1-42).

Per claims 2-3, current task data structure (page 258, left column, lines 35, Right Column, lines -21), context switch to execute the task (page 258, Right column, lines 33-59).

Per claim 4, first task control block includes a pointer data structure that contain a pointer to a location of the second task control block (stack register, Page 256, right col. Lines 35-42).

Per claims 5, and 15, the first area of the memory space is a system space (Fig. 1, ROM subsystem), and the second area of the memory is user state (Fig. 1, RAM subsystem).

Per claim 6, wherein the number of second task information data structures includes error status information for the task (Fig. 3, Event Queue, and wait/test/signal).

Per claim 7-8, wherein the number of second task information data structures includes a set of pointers to a set of standard modules for the task, and number of second

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task information data structures includes a pointer to environment variables for the task (call to the operating system elements from the applications software, and encoding system functions, Zero to 256, encoding one of the system functions page, 256, Right Column, lines 52-65).

Per claim 9-10, wherein the number of second task information data structures includes a pointer to context information for remote procedure calls made by the task (Fig. 3, Interrupt/Trap Handler, and context switch, and dispatch).

Per claim 11, and 19, wherein the number of second task information data structures includes a pointer to exception information (page 258, Right col., lines 47-64, interrupt/trap, and Event Queue).

Per claim 12, the system of claim 1, wherein the number of second task information data structures includes a user-definable spare field (Fig. 3, Even Manager, semaphore manager, and Create/Destroy).

Per claim 16, wherein the first task control block and the second task control blocks are located in a system space, the system space within the memory space (Fig. 1, ROM subsystem).

Per claim 13, a real-time operating system (Fig.1 Arcade game).

Per claim 20-21, wherein the first number of state information values are saved on an interrupt stack (Page 258, Right col. Lines 47-64).

5. Applicant on page 2-3 of his remarks argues:

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"Mateosian describes well known systems and processes for implementing a multi-process computing system - much of the description given by Mateosian is reflected in the Background Information portion of the Specification of the present application (see Specification, pp. 2-3). However, Mateosian provides no discussion about a task control block associated with a task, much less a task control block located in a memory space and including a number of task information data structures. Moreover, Mateosian does not describe a system task control block associated with a task, or a user task control block associated with the task, or task information that includes a pointer to the user task control block."

In response, it is submitted that the task control block located in memory stack and including a number of task information data structure is taught by Mateosian in Fig. 3, under process manager (See, create/destroy, suspend/resume, and ...). These are all data structures that are controlling tasks. Applicant should argue that these data structures are not on memory, and are not controlling tasks and finally are not data structure.

Later on pages 3-4, applicant reciting claims language and argues:

"Mateosian does not teach or suggest the system recited in claim 1. For example, Mateosian does not teach or suggest a first task control block associated with the task and located in a first memory space, and a second task control block associated with the task and located in a second area of the memory space. Mateosian further does not teach or suggest that the first area of the memory space is not directly accessible by the task and the second area of the memory space is directly accessible by the task. As a result, Applicant believes claim 1 to be patentable over Mateosian, and respectfully requests that the Examiner withdraw the rejection of claim 1. As claims 2-13 each depend (either directly or indirectly) from claim 1, and therefore include all of the elements of claim 1, Applicant believes claims 2-13 to be patentable over Mateosian as well, and respectfully requests that the Examiner withdraw the rejections of claims 2-13 as well".

## And on page 4 argues:

"As discussed above, Mateosian also does riot teach or suggest the method recited by claim 14. For example, Mateosian does not teach or suggest creating a first task control block for a task, or creating a second task control block for the task, or loading an address for the location of the second task control block into the first task control block. As a result, Applicant believes claim 14 to be patentable over Mateosian, and respectfully requests that the Examiner withdraw

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the rejection of claim 14. As claims 15 and 16 each depend from claim 14, and therefore include all of the elements of claim 14, Applicant believes claims 15 and 16 to be patentable over Mateosian as well, and respectfully requests that the Examiner withdraw the rejections of claims 15 and 16 as well".

In response, it is submitted that this is again a repeat of the claim language. Applicant's attention is directed to the rejection of claim under 35 USC 102 (b) *supra*. Sections of the first task control block (the top left corner block in Fig. 3, and of the second control block (the top row in fig. 3, middle block) which are different data structures depicted in Fig. 3, are on different part of the memory. Applicant should argue why they are not on different part of the memory. See the description of Fig. 3, i.e.: Operating system elements required by arcade game application, and all elements supports software functions. Those are block of software on the memory controlling an application.

## On page 4, applicant argues:

As discussed above, Mateosian does not teach or suggest all of the elements of claim 17. For example, Mateosian does not teach or suggest savings task information for a first task in a system task control block associated with the first task, the task information for the first task including a pointer to a user task control block associated with the first task, or loading task information for a second task from a system task control block associated with the second task, the task information for the second task including a pointer to a user task control block associated with the second task. As a result, Applicant believes claim 17 to be patentable over Mateosian, and respectfully requests that the Examiner withdraw the rejection of claim 17.

## And on page 5, argues:

"As discussed above, Mateosian does not teach or suggest all of the elements of claim 18. For example, saving a first number of state information values from a current task data structure for a currently executing task, the current task data structure including a pointer data structure holding a pointer to a second number

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of state information values. As a result, Applicant believes claim 18 to be patentable over Mateosian, and respectfully requests that the Examiner withdraw the rejection of claim 18. As claims 19-21 each depend from claim 18 (either directly or indirectly), and therefore include all of the elements of claim 18, Applicant believes claims 19-21 to be patentable over Mateosian as well, and respectfully requests that the Examiner withdraw the rejections of claims 19-21 as well".

In response, again applicant is reciting claim elements and argues the reference does not teach the claim. The 'context switching' is taught by Mateosian, in page 258, Right column under the title Context Switching. In there, he teaches saving the context of one process and recall the context of another process (See page 260, left column, lines 23-27, "A load Control register instruction allows the transfer of any of these registers to or from a general purpose register, permitting them to be saved and restored".

As noted by the Court of Customs and Patent Appeals, "argument cannot take the place of evidence." In re Langer, 503 F.2d 1380, 1395, 183 USPQ 288, 299 (CCPA 1974). In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). Applicants have not submitted sufficient evidence to rebut the strong prima facie case of obviousness established by Examiner. It is unclear why the context switching disclosed in Mateosian, is different from the one disclosed in the application.

As another example, the PSA pointers are taught by Mateosian on page 258, right columns last paragraph. (See also, Fig, 4, PSA pointers).

- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

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A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE The application has been amended as follows: ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is (703) 308-6903. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Majid Banankhah

1/12/04